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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,077	09/26/2000	Jenwei Hsieh	016295.0618	5720
7590	12/17/2004			EXAMINER DUONG, FRANK
Baker Botts LLP One Shell Plaza 910 Louisiana Houston, TX 77002-4995			ART UNIT 2666	PAPER NUMBER

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/670,077	HSIEH ET AL.
Examiner	Art Unit	
	Frank Duong	2666

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 July 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-24 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: ____.

DETAILED ACTION

1. This Office Action is a response to the amendment dated 07/15/04. Claims 1-24 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by *White Paper-Catalyst 8500 Architecture, Cisco, pages 1-19, 1998* (hereinafter "Doc1").

Regarding **claim 1**, in accordance with Doc1 entirety, Doc1 shows a switching system (*page 4, Figure 1; Catalyst 8500 and thereafter*) comprising:

a switch (*page 4, Figure 1; Catalyst 8500*) operable to communicatively couple a plurality of devices (*not shown; inherently there are devices coupled to Catalyst 8500 through line cards as depicted in Figure 4, on page 7*), wherein the switch is operable to receive a module (*(CEFA module depicted in Figure 5) or (SRP module disclosed on page 9 and thereafter)*), wherein the module comprises one or more module routing components (*description of Line Card Architecture on page 7 and thereafter or description of SRP on page 9 and thereafter*) operable to communicatively couple the devices when the module is received by the switch (*page 4, right column, second paragraph and thereafter*).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Doc1 further shows wherein the switch further comprises one or more intermediate routing components (CEFA) operable to communicatively couple with the module routing components (SRP) when the module is received by the switch (see *Figure 1 for the connections between Line Cards and Route Processor and the corresponding description pertaining Route Processor discussed on page 4, right column, last paragraph and thereafter*).

Regarding **claim 3**, in addition to features recited in base claim 2 (see rationales discussed above), Doc1 further shows wherein the module routing components (SRP) are the same type as the intermediate routing component (CEFA) (*page 4, right column last paragraph; Doc1 discloses the Processor Engine is responsible for all address and route learning and distribution by maintaining all Layer 3 routes and Layer 2 MAC addresses and so are CEFA as disclosed on page 4, right column, second paragraph*).

Regarding **claim 4**, in addition to features recited in base claim 2 (see rationales discussed above), Doc1 further shows wherein the intermediate routing components (CEFA) and module routing components (SRP) are ASIC-based routing components (*page 2, right column, second paragraph or page 4, right column, second paragraph and thereafter*).

Regarding **claim 5**, in addition to features recited in base claim 2 (see rationales discussed above), Doc1 further shows wherein the number of module routing components (SRPs) is equal to half the number of intermediate routing components (CEFAs) (*Figure 1 on page 4 depicted 4 Line Card modules and one RSP module*).

However, on page 2, left column, second paragraph, it is provided in Catalyst switch with a second, redundant SRP module. Thus, the ratio between RSP module and the CEFA modules is one half as claimed).

Regarding **claim 6**, in addition to features recited in base claim 1 (see rationales discussed above), Doc1 further shows wherein the switch is operable to receive a plurality of modules (Figure 4; Line Cards).

Regarding **claim 7**, in accordance with Doc1 entirety, Doc1 shows a network switch (page 4, Figure 1; Catalyst 8500 and thereafter) operable to communicatively couple a plurality of devices (not shown; inherently there are devices coupled to Catalyst 8500 through line cards as depicted in Figure 4, on page 7) attached to a computer network (Figure 4), wherein the switch is operable to receive a module ((CEFA module depicted in Figure 5) or (SRP module disclosed on page 9 and thereafter)), wherein the network switch (Fig. 1) comprises a module interface (Fabric Interface) operable to receive a module (Line Card), wherein the module comprises one or more module routing components (CEF ASICs) (description of Line Card Architecture on page 7 and thereafter or description of SRP on page 9 and thereafter) operable to communicatively couple the devices when the module is received by the switch (page 4, right column, second paragraph and thereafter).

Regarding **claim 8**, in addition to features recited in base claim 7 (see rationales discussed above), Doc1 further shows one or more intermediate routing components (CEFA) operable to communicatively couple with the module routing components (SRP) when the module is received by the switch (see Figure 1 for the connections between

Line Cards and Route Processor and the corresponding description pertaining Route Processor discussed on page 4, right column, last paragraph and thereafter).

Regarding **claim 9**, in addition to features recited in base claim 8 (see rationales discussed above), Doc1 further shows wherein the module routing components (SRP) are the same type as the intermediate routing component (CEFA) (*page 4, right column last paragraph; Doc1 discloses the Processor Engine is responsible for all address and route learning and distribution by maintaining all Layer 3 routes and Layer 2 MAC addresses and so are CEFA as disclosed on page 4, right column, second paragraph*).

Regarding **claim 10**, in addition to features recited in base claim 8 (see rationales discussed above), Doc1 further shows wherein the intermediate routing components (CEFA) and module routing components (SRP) are ASIC-based routing components (*page 2, right column, second paragraph or page 4, right column, second paragraph and thereafter*).

Regarding **claim 11**, in addition to features recited in base claim 8 (see rationales discussed above), Doc1 further shows wherein the number of module routing components (SRPs) is equal to half the number of intermediate routing components (CEFAs) (*Figure 1 on page 4 depicted 4 Line Card modules and one RSP module. However, on page 2, left column, second paragraph, it is provided in Catalyst switch with a second, redundant SRP module. Thus, the ratio between RSP module and the CEFA modules is one half as claimed*).

Regarding **claim 12**, in addition to features recited in base claim 7 (see rationales discussed above), Doc1 further shows wherein the switch is operable to receive a plurality of modules (Figure 1; Line Cards).

Regarding **claim 13**, in accordance with Doc1 entirety, Doc1 shows a module (Figure 1; Line Card) operable to be received by a network switch (Figure 1) operable to communicatively couple a plurality of devices attached to a computer network (Figure 4), wherein the module comprises one or more module routing components (CEF ASICs) (*description of Line Card Architecture on page 7 and thereafter or description of SRP on page 9 and thereafter*) operable to communicatively couple the devices when the module is received by the switch (*page 4, right column, second paragraph and thereafter*).

Regarding **claim 14**, in addition to features recited in base claim 13 (see rationales discussed above), Doc1 further shows wherein the network switch (Figure 1) further comprises one or more intermediate routing components (CEFA) operable to communicatively couple with the module routing components (SRP) when the module is received by the switch (*see Figure 1 for the connections between Line Cards and Route Processor and the corresponding description pertaining Route Processor discussed on page 4, right column, last paragraph and thereafter*).

Regarding **claim 15**, in addition to features recited in base claim 14 (see rationales discussed above), Doc1 further shows wherein the module routing components (SRP) are the same type as the intermediate routing component (CEFA) (*page 4, right column last paragraph; Doc1 discloses the Processor Engine is*

responsible for all address and route learning and distribution by maintaining all Layer 3 routes and Layer 2 MAC addresses and so are CEFA as disclosed on page 4, right column, second paragraph).

Regarding **claim 16**, in addition to features recited in base claim 14 (see rationales discussed above), Doc1 further shows wherein the intermediate routing components (CEFA) and module routing components (SRP) are ASIC-based routing components (*page 2, right column, second paragraph or page 4, right column, second paragraph and thereafter*).

Regarding **claim 17**, in addition to features recited in base claim 14 (see rationales discussed above), Doc1 further shows wherein the number of module routing components (SRPs) is equal to half the number of intermediate routing components (CEFAs) (*Figure 1 on page 4 depicted 4 Line Card modules and one RSP module. However, on page 2, left column, second paragraph, it is provided in Catalyst switch with a second, redundant SRP module. Thus, the ratio between RSP module and the CEFA modules is one half as claimed*).

Regarding **claim 18**, in addition to features recited in base claim 14 (see rationales discussed above), Doc1 further shows wherein the network switch is operable to receive a plurality of modules (*Figure 1; Line Cards*).

Regarding **claim 19**, in accordance with Doc1 entirety, Doc1 discloses a method for upgrading the bisectional bandwidth (*page 4, Figure 1; Catalyst 8500 and thereafter*) of a network comprising a plurality of devices (Figure 4), comprising the steps of:

providing a network switch (*page 4, Figure 1; Catalyst 8500 and thereafter*) operable to communicatively couple a plurality of devices (*not shown; inherently there are devices coupled to Catalyst 8500 through line cards as depicted in Figure 4, on page 7*) attached to a computer network (Figure 4), wherein the network switch (Fig. 1 or Fig. 5) comprises a module interface (Fabric Interface) operable to receive a module (Line Card);

providing a module (Line Card) comprises one or more module routing components (CEF ASICs) (*description of Line Card Architecture on page 7 and thereafter or description of SRP on page 9 and thereafter*) operable to communicatively couple the devices when the module is received by the switch (*page 4, right column, second paragraph and thereafter*); and

receiving the module (Line Card connected in the switch of Figure 1 or Figure 5).

Regarding **claim 20**, in addition to features recited in base claim 19 (see rationales discussed above), Doc1 further discloses wherein the network switch further comprises one or more intermediate routing components (CEFA) operable to communicatively couple with the module routing components (SRP) when the module is received by the switch (*see Figure 1 for the connections between Line Cards and Route Processor and the corresponding description pertaining Route Processor discussed on page 4, right column, last paragraph and thereafter*).

Regarding **claim 21**, in addition to features recited in base claim 20 (see rationales discussed above), Doc1 further shows wherein the module routing components (SRP) are the same type as the intermediate routing component (CEFA)

(page 4, right column last paragraph; Doc1 discloses the Processor Engine is responsible for all address and route learning and distribution by maintaining all Layer 3 routes and Layer 2 MAC addresses and so are CEFA as disclosed on page 4, right column, second paragraph).

Regarding **claim 22**, in addition to features recited in base claim 20 (see rationales discussed above), Doc1 further shows wherein the intermediate routing components (CEFA) and module routing components (SRP) are ASIC-based routing components (*page 2, right column, second paragraph or page 4, right column, second paragraph and thereafter*).

Regarding **claim 23**, in addition to features recited in base claim 20 (see rationales discussed above), Doc1 further shows wherein the number of module routing components (SRPs) is equal to half the number of intermediate routing components (CEFAs) (*Figure 1 on page 4 depicted 4 Line Card modules and one RSP module. However, on page 2, left column, second paragraph, it is provided in Catalyst switch with a second, redundant SRP module. Thus, the ratio between RSP module and the CEFA modules is one half as claimed*).

Regarding **claim 24**, in addition to features recited in base claim 19 (see rationales discussed above), Doc1 further shows wherein the network switch is operable to receive a plurality of modules (Figure 4; Line Cards).

Response to Arguments

3. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shifting the routing functionality to a line card using application-specific integrated circuits (ASICs) to speed up the routing process is well known and disclosed in the following references. Examiner reserves the right to apply the below reference in a next Office Action should the Applicants, in a response to this Office Action, amend the claims to overcome the applied art.

Dobbins et al (USP 5,485,455).

Civanlar et al (USP 56,078,963).

Flanders et al (USP 6,172,980).

Hebb et al (USP 6,463,067).

Decasper et al (Router Plugins-A Software Architecture for Next Generation Routers, ACM, pages 229-240, 1998).

Aweya (IP Router Architecture: An Overview,

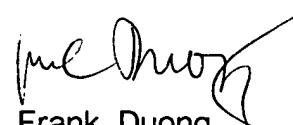
<http://citeseer.ist.psu.edu/aweya99ip.html>, pages 1-48, 1999.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is (571) 272-3164. The examiner can normally be reached on 7:00AM-3:30PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Frank Duong
Examiner
Art Unit 2666

December 12, 2004